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Parameter Optimization Performance Analysis of 4-Bit CMOS Layout for Adder

Prof. Sandip Nimade
Department of ECE
Technocrats Institute of Science and Technology, Bhopal

Amrita Shukla
Department of ECE
Technocrats Institute of Science and Technology, Bhopal
E-mail: amrita.shukla87@gmail.com

Prof. Vikas Gupta
Department of ECE
Technocrats Institute of Science and Technology, Bhopal

***Abstract* – This paper we design 4-bit CMOS layout for 4-bit full adder with the help of half adder and other logic gates. In this paper we calculate power dissipation of gates and modules which we used in designing and also calculate the no. of transistors which were used in designing of gates. The result of simulation of adder layout is in Microwind2.**

***Keywords* – X-OR, Tox, Full Adder, VLSI, Microwind 2.**

I. INTRODUCTION

A full adder is a combinational circuit that performs the arithmetic sum of three bits: A, B and a carry in, C, from a previous addition, Fig. 1. Also, as in the case of the half adder, the full adder produces the corresponding sum, S, and a carry out Co. As mentioned previously a full adder maybe designed by two half adders in series as shown below in Figure… The sum of A and B are fed to a second half adder, which then adds it to the carry in C (from a previous addition operation) to generate the final sum S. The carry out, Co, is the result of an OR operation taken from the carry outs of both half adders.

$$S = x'y'z + x'yz' + xy'z + xyz$$

$$S = x \oplus y \oplus z$$

$$C = x'yz + xy'z + xyz' + xyz$$

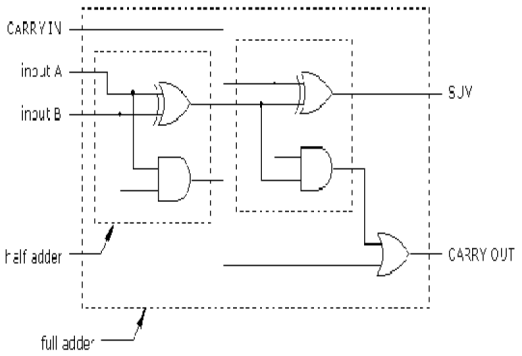

Fig.1. Full Adder

Full adder can be constructed using two X-OR gates, two AND gates and an OR gate as shown in the Fig.1.

II. REALIZATION OF GATE LAYOUT

A. *Realization of a CMOS XOR Gate*

This gate is designed with the help of a X-NOR gate and an inverter. Output of a X-NOR gate is feed to an inverter so that we can get the output of X-OR gate. The layout of a XOR gate is shown in fig.2

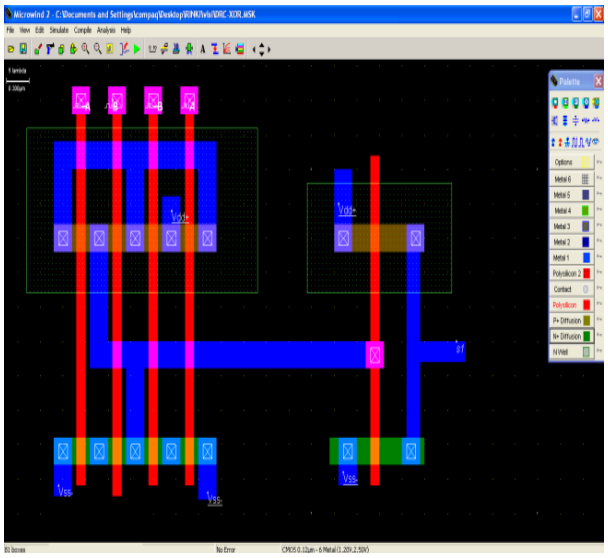

Fig.2. CMOS X-OR gate

The Simulation result of CMOS X-OR gate as shown in figure 3.

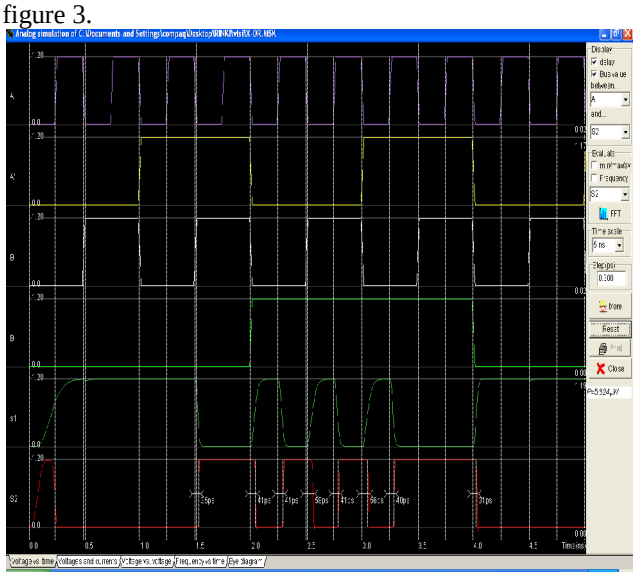

Fig.3. Simulation of X-OR gate

B. *Realization of a CMOS AND Gate*

This gate is designed with the help of a AND gate and an inverter. Output of a AND gate is feed to an inverter so that we can get the output of AND gate. The layout of a AND gate is shown in fig.4.

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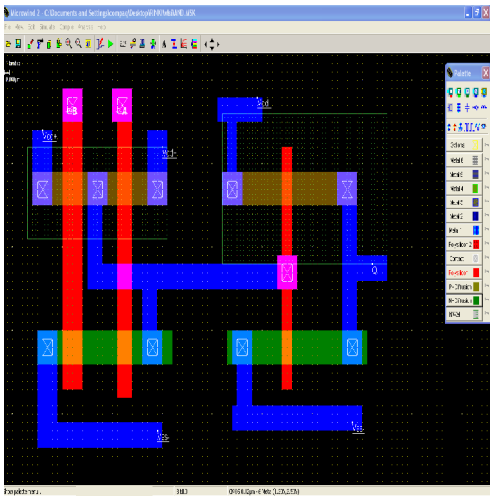

Fig.4. CMOS AND gate

The Simulation result of CMOS AND gate shown in figure 5.

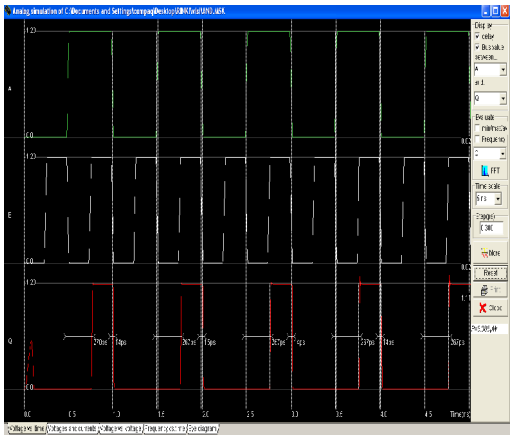

Fig.5. simulation of AND gate

C. *Realization of Half Adder*

This module is designed with the help of a X-OR gate & an AND gate. Output of a X-OR output gate is represents as SUM output and output of AND gate is represents CARRY output.

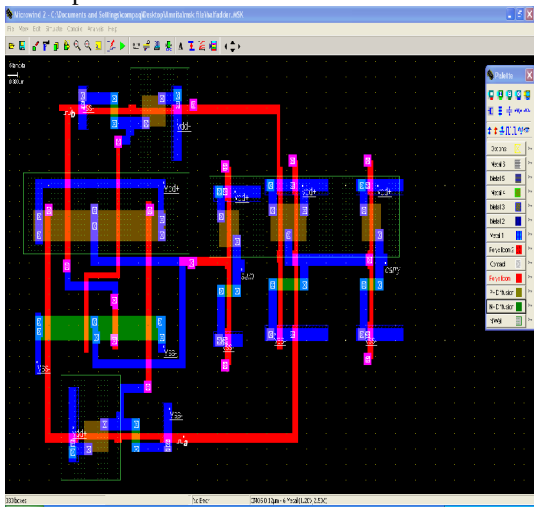

Fig.6. CMOS Half Adder

The simulation results of Half Adder is shown in figure 7.

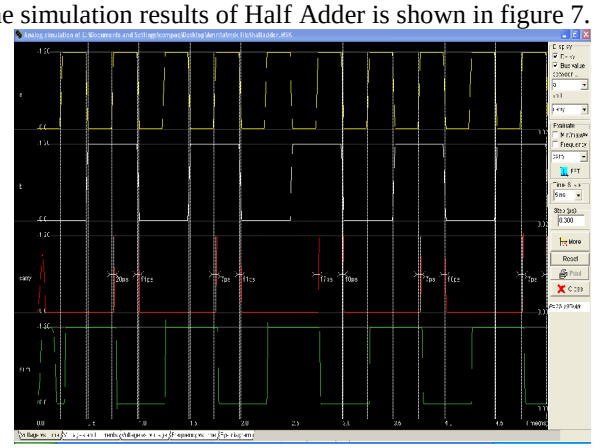

Fig.7. Half Adder simulation

D. *Realization of Full Adder*

This module is designed with the help of two Half Adder and OR gate. Output of a gate is represents as SUM output and CARRY output.

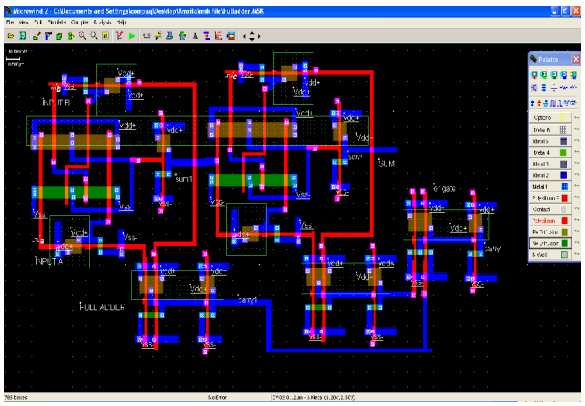

Fig.8. CMOS Full Adder

The simulation results of Full Adder is shown in figure 9.

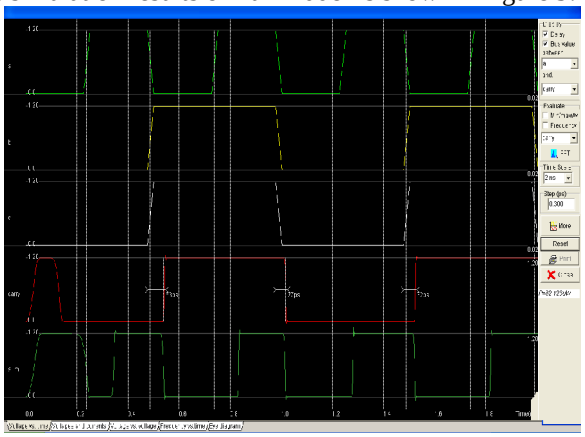

Fig.9. Simulation of Full Adder

E. *Realization of 4-bit Adder*

This module is designed with the help of Full Adder which is connected in parallel .Output of a gate is represents as SUM output and CARRY output.

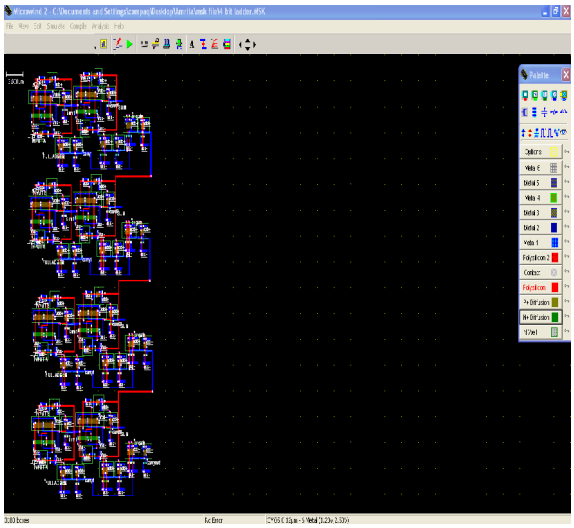

Fig.10. CMOS 4-bit Adder

The simulation result is shown in figure 11.

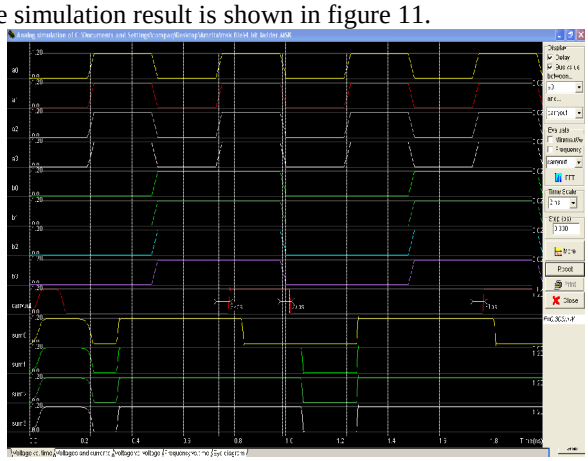

Fig.11. Simulation of 4-bit ADDER

III. RESULT

Table 1: Detail comparison of Gates and Module for different parameter

CMOS Logic	Number of transistor	Ids current	Power dissipation
	5NMOS 5 PMOS	0.236mA	3.088µW
X-OR	7 NMOS 7 PMOS	0.087mA	5.824 µW
Half adder	10NMOS 10 PMOS	0.269mA	46.248µW
Full adder	23NMOS 23 PMOS	0.206mA	70.80µW
4 bit adder	92NMOS 92 PMOS	0.256mA	0.255mW

Table No.1 shows that AND gate can be made with the help of 5 nmos and 5 pmos with i_{ds} =0.236mA and power dissipation is 3.088 µW with 1.2V power supply. similarly X-OR gate contain 7nmos and 7 pmos with dissipation of 5.824 µW and i_{ds} 0.087mA. In half adder 10 nmos and 10 pmos is used and we get i_{ds} 0.269mA and 46.248 µW power dissipation. Full adder contain 23 nmos and 23pmos with dissipation of 70.80 µW and i_{ds} is 0.206mA, and 4 bit adder contain 92nmos and 92pmos with i_{ds} 0.256mA and power dissipation of 0.255mW with supply voltage of 1.2v.

IV. CONCLUSION

This table no.1 calculate some parameter like I_{ds} and power dissipation for different gates and modules. We also calculate the no. of transistors used in CMOS layout. As can see that with the increase of module and transistor current and dissipation also increases.

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AUTHOR'S PROFILE

Amrita Shukla
Received her B.E. from Thakral College of Technology, Bhopal. She ispursuing M. Tech. in Micro Electronics & VLSI Design, Technocrats Institute of Technology (Bhopal).
E-mail : amrita.shukla87@gmail.com

Prof. Sandip Nimade
Assistant Professor
B.E., M.Tech in Micro Electronics & VLSI Design Electronics & Communication Engineering Department Technocrats Institute of Science and Technology, Bhopal.

Prof. Vikas Gupta
Assistant Professor
B.E., M.Tech in Digital Communication Pursuing Ph.D. from MANIT, Bhopal Electronics & Communication Engineering Department. Technocrats Institute of Science and Technology, Bhopal.